WHAT IS CLAIMED IS:

1. A method of writing to a memory comprising:

receiving an address portion comprising a first number of bits;

blocking a second number of bits of the address portion, the second number less than the first number;

passing a third number of bits of the address portion, wherein the second number summed with the third number is equal to the first number;

decoding the third number of bits to select a fourth number of memory cells, the fourth number equal to two to the power of the second number;

receiving a fourth number of data bits; and

writing the fourth number of data bits to the fourth number of memory cells.

2. The method of claim 1 further comprising:

after receiving a fourth number of data bits, multiplexing the fourth number of data bits to the selected fourth number of memory cells.

3. The method of claim 2 wherein the memory is a dual port memory.

4. A method of reading from a memory comprising:

receiving an address portion comprising a first number of bits;

blocking a second number of bits of the address portion, the second number less than the first number;

passing a third number of bits of the address portion, wherein the third number summed with the second number is equal to the first number;

reading a fourth number of data bits from a fourth number of memory cells; and

decoding the third number of bits to multiplex a fifth number of data bits to a fifth number of outputs.

5. The method of claim 4 wherein the fifth number is equal to two to the power of the second number.

6. The method of claim 5 wherein the memory is a dual port memory.

7. An integrated circuit comprising:

an address conforming logic block configured to receive a first number of address bits, block a second number of address bits, and pass a third number of address bits;

an address decoder coupled to the address conforming logic block configured to decode the third number of address bits and provide a fourth number of column select signals; and

a memory array having memory cells arranged in rows and columns, configured to receive the fourth number of column select signals.

8. The integrated circuit of claim 7 wherein the second number summed with the third number is equal to the first number.

9. The integrated circuit of claim 8 wherein the fourth number is equal to two to the power of the second number.

10. The integrated circuit of claim 8 wherein the fourth number is equal to a fifth number multiplied by two to the power of the second number.

11. The integrated circuit of claim 7 further comprising:

a multiplexer circuit configured to receive a fourth number of data bits and the fourth number of column select signals,

wherein the fourth number of column select signals selects a fourth number of columns in the memory array, and the multiplexer circuit multiplexes the fourth number of data bits to the fourth number of columns in the memory array.

12. The integrated circuit of claim 11 further comprising:

a configuration memory having a plurality of storage cells for storing a plurality of configuration bits,

wherein the plurality of configuration bits is used to determine the second number and the third number.

13. The integrated circuit of claim 11 wherein the integrated circuit is a programmable logic device.

14. An integrated circuit comprising:

an address conforming logic block configured to receive a first number of address bits, block a second number of address bits, and pass a third number of address bits;

an address decoder coupled to the address conforming logic block configured to decode the third number of address bits and provide a fourth number of column select signals;

a memory array having memory cells arranged in rows and a fifth number of columns; and

a fifth number of sense amplifiers coupled to the memory array, configured to provide a fifth number of read data bits.

15. The integrated circuit of claim 14 further comprising:

a multiplexing circuit coupled to the address decoder and the fifth number of sense amplifiers, configured to receive the fourth number of column select signals and the fifth number of read data bits, and multiplex a fourth number of read data bits to a fourth number of outputs.

16. The integrated circuit of claim 15 wherein each of the fifth number of sense amplifiers is coupled to one of the fifth number of columns in the memory array.

17. The integrated circuit of claim 16 further comprising:

a plurality of storage cells configured to store a plurality of configuration bits,

wherein the plurality of configuration bits is used to determine the second number and the third number.

18. The integrated circuit of claim 15 wherein the second number summed with the third number is equal to the first number.

19. The integrated circuit of claim 15 wherein the fourth number is equal to two to the power of the second number.

20. The integrated circuit of claim 15 wherein the fourth number is equal to a fifth number multiplied by two to the power of the second number.

21. The integrated circuit of claim 17 wherein the integrated circuit is a programmable logic device.

22. An integrated circuit comprising:

a memory array having a plurality of memory cells arranged in rows and columns;

address configuration means for receiving a plurality of address bits comprising a first portion of address bits and a second portion of address bits, blocking the first portion of address bits, and providing the second portion of address bits;

address decoder means for receiving the second portion of address bits and providing a plurality of select lines, wherein the plurality of select lines selects a plurality of columns of memory cells in the memory array; and

data multiplexer means for receiving a plurality of data bits and the plurality of select lines, and multiplexing the plurality of data bits to the plurality of columns of memory cells in the memory array.

23. The integrated circuit of claim 22 wherein the first portion of address bits comprises a first number of address bits, the second portion of address bits comprises a second number of address bits, and the plurality of selected columns of memory cells in the memory array comprises a third number of selected columns of memory cells in the memory array, and

wherein the third number is equal to a fourth number multiplied by two to the power of the first number.

24. The integrated circuit of claim 22 wherein the first portion of address bits comprises a first number of address bits, the second portion of address bits comprises a second number of address bits, and the plurality of selected columns of memory cells in the memory array comprises a third number of selected columns of memory cells in the memory array, and

wherein the third number is equal to two to the power of the first number.

25. An integrated circuit comprising:

a memory array having a plurality of memory cells arranged in rows and columns;

sense amplifier means for reading data from the columns of memory cells in the memory array and providing a plurality of read data bits;

address configuration means for receiving a plurality of address bits comprising a first portion of address bits and a second portion of address bits, blocking the first portion of address bits, and providing the second portion of address bits;

address decoder means for receiving the second portion of address bits and providing a plurality of select lines; and

data multiplexer means for receiving the plurality of read data bits and the plurality of select lines, and multiplexing a first portion of the plurality of read data bits to a plurality of output data lines.

26. The integrated circuit of claim 25 wherein the first portion of address bits comprises a first number of address bits, the second portion of address bits comprises a second number of address bits, and the first portion of the plurality of read data bits comprises a third number of read data bits, and

wherein the third number is equal to a fourth number multiplied by two to the power of the first number.

27. The integrated circuit of claim 25 wherein the first portion of address bits comprises a first number of address bits, the second portion of address bits comprises a second number of address bits, and the first portion of the plurality of read data bits comprises a third number of read data bits, and

wherein the third number is equal to two to the power of the first number.